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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,734	11/20/2000	Vincent K. Chan	0100.0100120	7999
24228	7590	03/21/2003		
MARKISON & RECKAMP, PC PO BOX 06229 WACKER DR CHICAGO, IL 60606-0229			EXAMINER	
			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	
			DATE MAILED: 03/21/2003	10

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/716,734	CHAN ET AL.
	Examiner	Art Unit
	Alexander O Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 January 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) 10,11,13-16,18-20 and 24-27 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-9,12,17 and 21-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

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Art Unit: 2826

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Serial Number: 09/716734 Attorney's Docket #: 0100.0100120
Filing Date: 11/20/00;

Applicant: Chan et al.

Examiner: Alexander Williams

Applicant's election of Species I with traverse (claims 1-9, 12, 17 and 21-23) in Paper # 9, filed 1/13/03, has been acknowledged.

Applicant's arguments begins on page 1 to 3 are not to be persuasive. Applicant's argument begins on page 2, beginning of the third paragraph to the end of the first paragragh on page is not found to be persuasive. The technology of processing a silicon, gallium arsenide, silicon germanium or organic substrates are far different. In the examination of claims the Examiner would be interested in searching for the final structure of the semiconductor device claimed of each substrate. Therefore, the different substrates would require a search in different areas of technology. The Examiner would be unduly burdened to evaluate all claims fully on their merit at the full time. This is not found persuasive because of the reasons detailed in the last Office action.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 10, 11, 13-16, 18-20 and 24-27 drawn to an invention non-elected with traverse in Paper No. 9. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-9, 12 and 17 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lai et al. (U.S. Patent # 6,236,568 B1).

For example, in claim 1, Lai et al. (figures 1 to 4) specifically figure 2 show an integrated circuit package **1** comprising: a first substrate **3** having a first surface and a second surface, the first substrate including at least one heat generating circuit (**inherit**) and having a first coefficient of thermal expansion; and a second substrate **5** having at least a first surface and a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled (**by 6**) to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat generating circuit away from the at least one heat-generating circuit.

2. The Integrated Circuit package of claim 1, Lai et al.'s second substrate has a second surface, the integrated circuit package further comprising: a metallic heat sink **4** thermally coupled to the second surface of the second substrate, wherein a coefficient

of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

3. The integrated circuit package of claim 1, Lao et al.'s coupling between the metallic heat sink and the second substrate is such as to accommodate movement of the metallic heat sink with respect to the second substrate.

4. The Integrated circuit package of claim 2, Lao et al.'s coefficient of thermal expansion of the metallic heat sink is approximately seven times greater than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

5. The integrated circuit package of claim 1, Lao et al. further comprising: an adhesive layer **6** having a first surface and a second surface, the first surface of the adhesive layer being physically connected to the second surface of the first substrate, the second surface of the adhesive layer being physically connected to the first surface of the second substrate, wherein a thickness of the adhesive layer is less than or equal to approximately one-sixth of a thickness of the first substrate and wherein the adhesive layer functions to thermally couple the first substrate to the second substrate and to position the second Substrate in a fixed relation with respect to the first substrate.

6. The integrated circuit package of claim 1, Lao et al. further comprising: a printed circuit board substrate **2** having at least a first surface, the printed circuit board substrate including at least one conductive trace **22**; an adhesive layer **7** having a first surface and a second surface, the first surface of the adhesive layer being physically connected to the first surface of the printed circuit board substrate, the second surface of the adhesive layer being physically connected to the first surface of the first substrate, wherein the adhesive layer functions to at least position the first substrate in a fixed relation with respect to the printed circuit board substrate; and at least one electrically conductive path connecting the at least one heat-generating circuit to the at least one conductive trace.

7. The Integrated circuit package of claim 6, Lao et al.'s adhesive layer **7** comprises a conductive epoxy (silver paste).

8. The integrated circuit package of claim 6, Lao et al.'s at least one electrically conductive path comprises at least one wire bond **8**.

9. The integrated circuit package of claim 1, Lao et al.'s thickness of the second substrate **5** is greater than a thickness of the first substrate **3**.

12. The integrated circuit package of claim 1, Lao et al.'s first substrate comprises a

first semiconductor material and wherein the second substrate comprises one of the first semiconductor material and a second semiconductor material.

17. Lai et al. (figures 1 to 4) specifically figure 2 show an integrated circuit package **1** comprising: a first substrate **3** having a first surface and a second surface, the first substrate including at least one heat-generating circuit and having a first coefficient of thermal expansion, a second substrate **5** having a first surface and a second surface, the second substrate having a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat-generating circuit away from the at least one heat-generating circuit; a printed circuit board substrate **2** having at least a first surface, the printed circuit board substrate including at least one conductive trace; a first adhesive layer **6** having a first surface and a second surface, the first surface of the first adhesive layer being physically connected to the second surface of the first substrate, the second surface of the first adhesive layer being physically connected to the first surface of the second substrate, wherein a thickness of the first adhesive layer is less than or equal to approximately one-sixth of a thickness of the first substrate and wherein the first adhesive layer functions to thermally couple the first substrate to the second substrate and to position the second substrate in a fixed relation with respect to the first substrate; a second adhesive layer **7** having a first surface and a second surface, the first surface of the second adhesive layer being physically connected to the first surface of the printed circuit board substrate, the second surface of the second adhesive layer being physically connected to the first surface of the first substrate, wherein the second adhesive layer functions to at least position the first substrate in a fixed relation with respect to the printed circuit board substrate; at least one electrically conductive path connecting the at least one heat-generating circuit to the at least one conductive trace; and a metallic heat sink thermally **4** coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

Claims 21 to 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai et al. (U.S. Patent # 6,236,568 B1).

For example, in claim 1, Lai et al. (figures 1 to 4) specifically figure 2 show an integrated circuit package **1** comprising: a first substrate **3** having a first surface and a second surface, the first substrate including at least one heat generating circuit (**inherit**) and having a first coefficient of thermal expansion; and a second substrate **5** having at least a first surface and a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled (**by 6**) to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat generating circuit away from the at least one heat-generating circuit, but fail to explicitly show the method for fabricating an integrated circuit. However, it would be obvious to one of ordinary skill in the art to use the teaching of Lao et al.'s heat dissipating structure for an integrated circuit package to form the method for fabricating an integrated circuit of the purpose of preventing the encapsulant to cause a large thermal compressive stress on the integrated circuit chip during the cooling process.

22. The method of claim 21, Lai et al.'s second substrate has a second surface, the integrated circuit package further comprising: a metallic heat sink **4** thermally coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

23. The integrated circuit package of claim 21, Lao et al.'s first substrate comprises a first semiconductor material and wherein the second substrate comprises one of the first semiconductor material and a second semiconductor material.

Therefore, it would have been obvious to one of ordinary skill in the art to use the teaching of Lai et al.'s 's heat dissipating structure for an integrated circuit package to form the method for fabricating an integrated circuit claimed by Applicant of the purpose of preventing the encapsulant to cause a large thermal compressive stress on the integrated circuit chip during the cooling process.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/712,710,704,712,713,717,720,723,685,686,684,796, 784,786,787,777,778,734,737,738 361/702-704,717,718,715 165/20.3	3/17/03
Other Documentation: foreign patents and literature in 257/712,710,704,712,713,717,720,723,685,686,684,796, 784,786,787,777,778,734,737,738 361/702-704,717,718,715 165/20.3	3/17/03
Electronic data base(s): U.S. Patents EAST	3/17/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to **Examiner Alexander Williams** whose telephone number is (703) 308-4863.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center 2800 receptionist** whose telephone number is **(703) 308-0956**.

3/18/03



Primary Examiner
Alexander O. Williams